

ATM Network

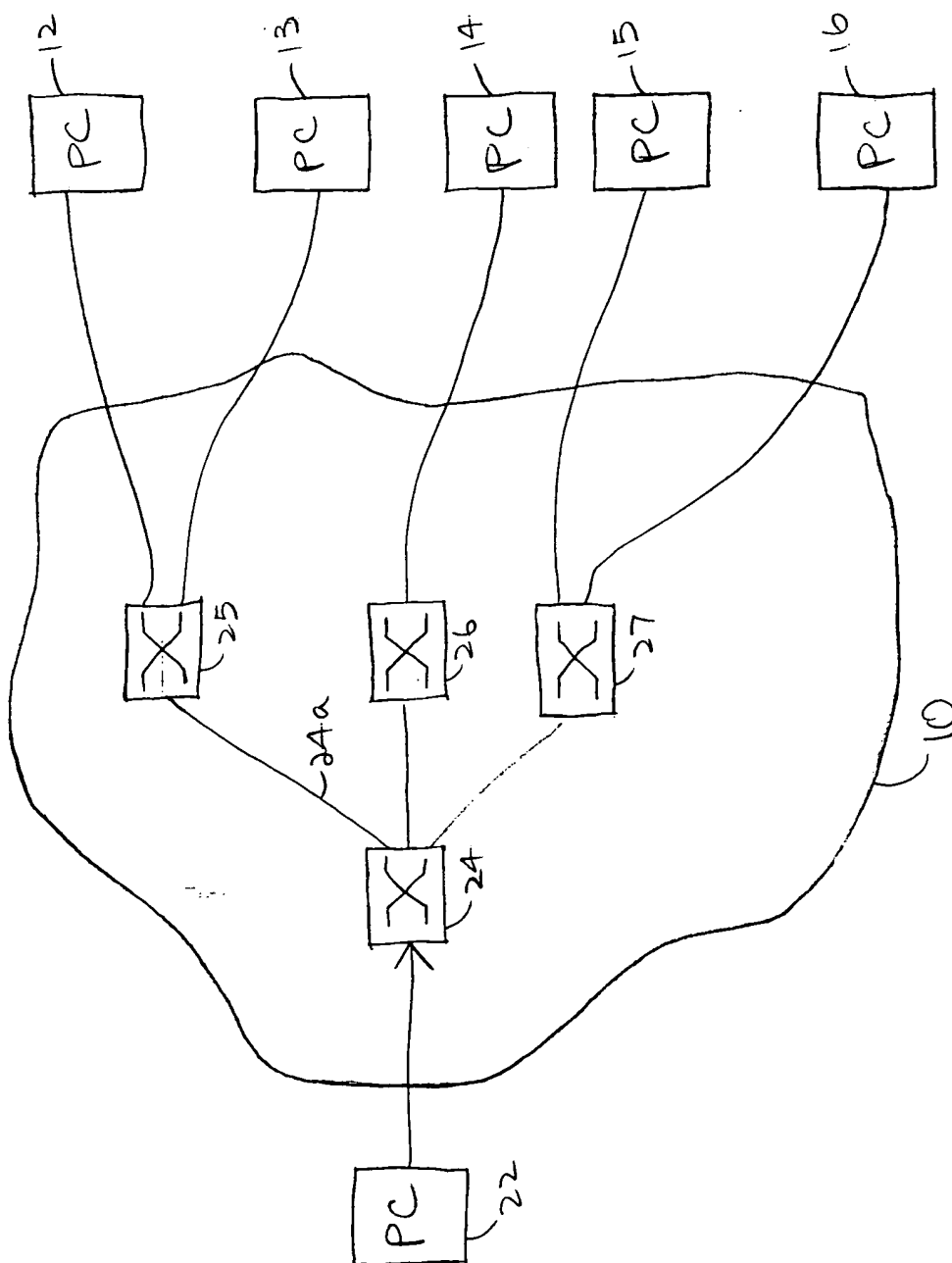


Fig. 1

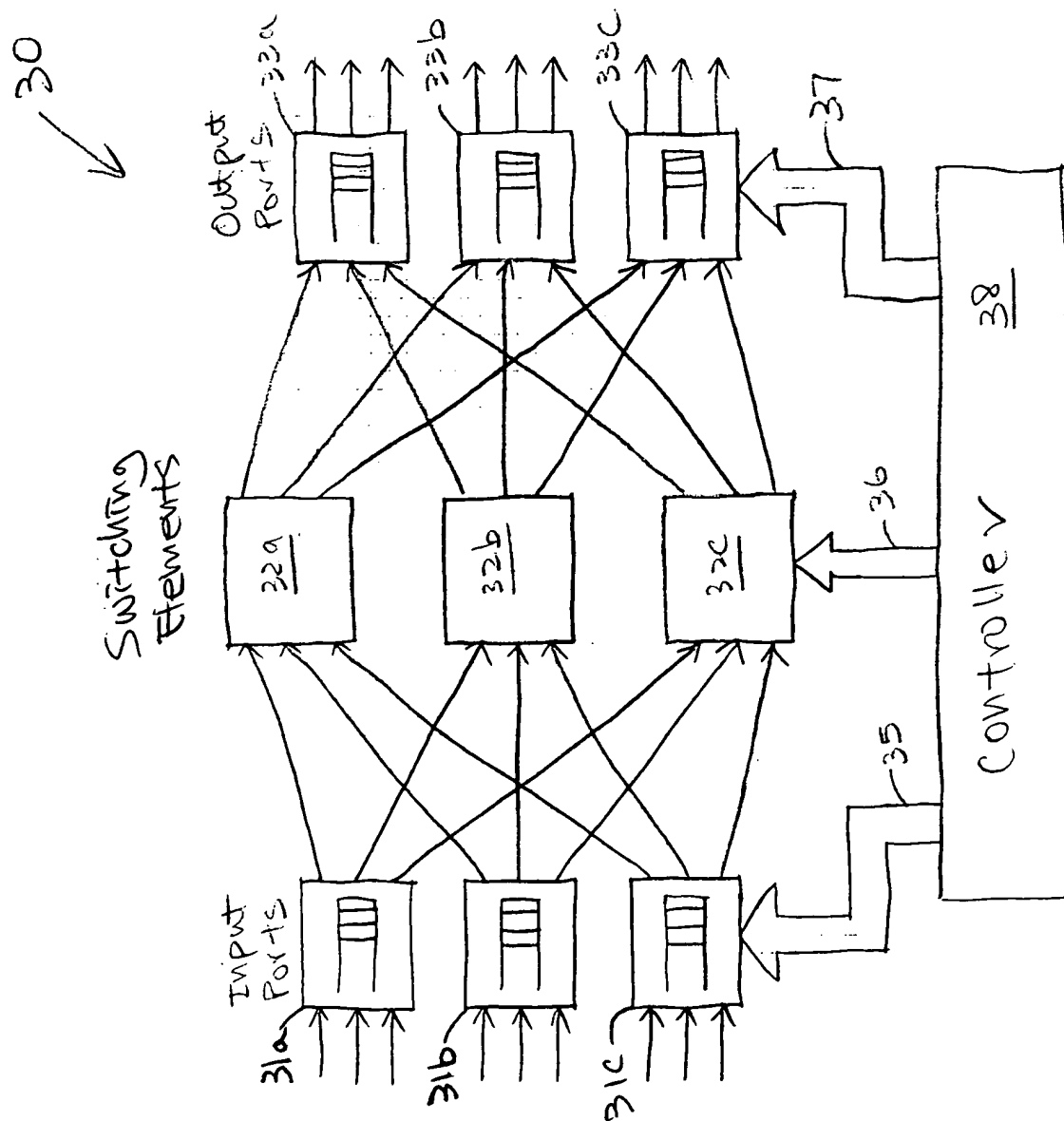


Fig. 2

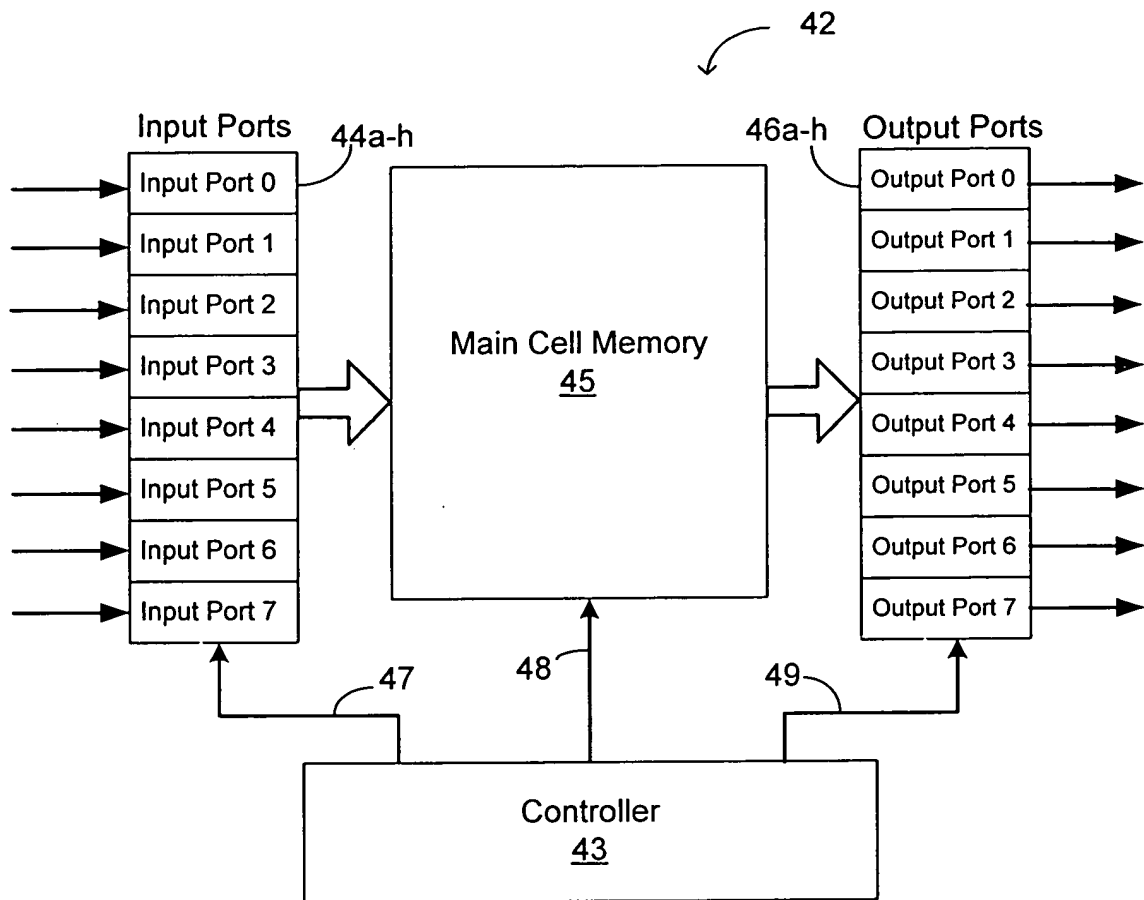


Figure 3

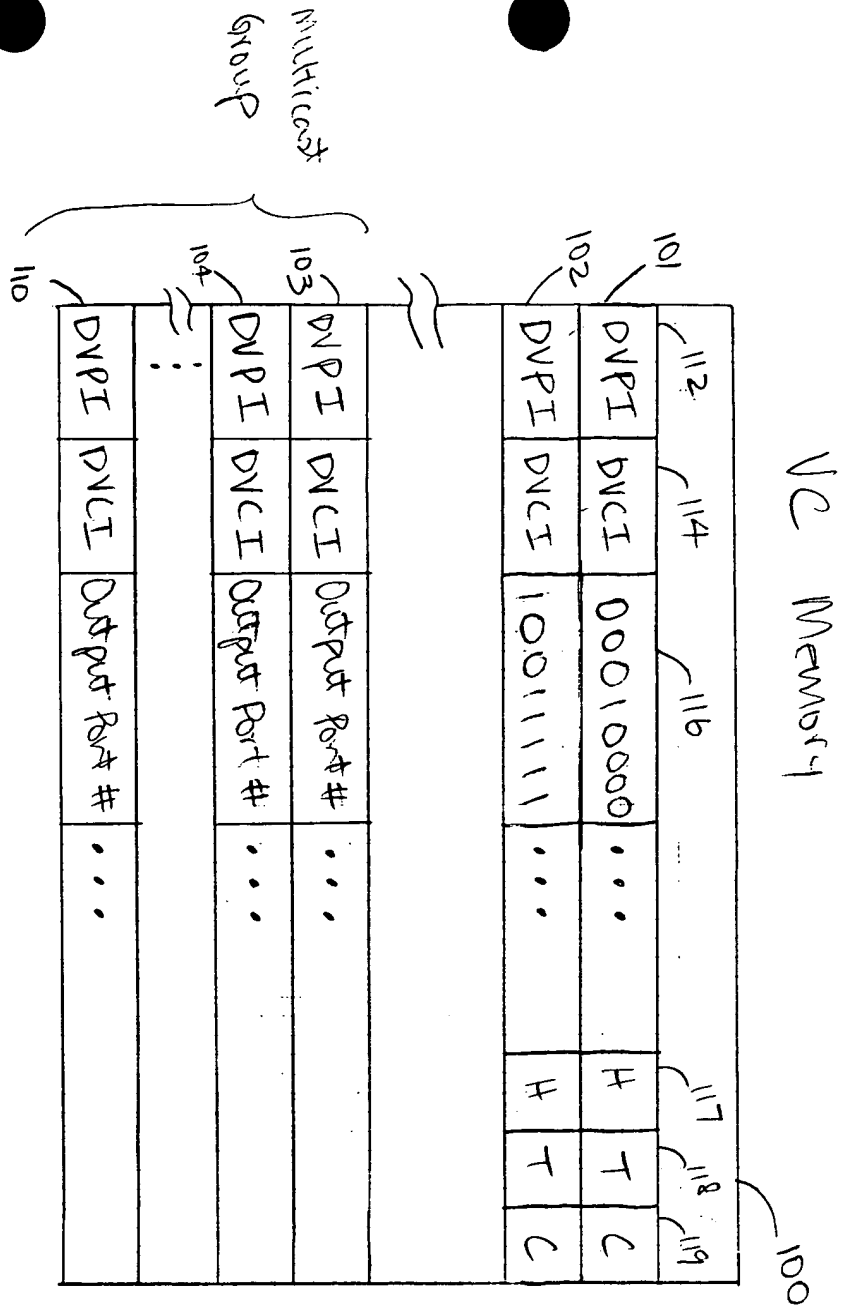


Fig. 4

FIG. 4 is a schematic diagram of a VC memory structure. The structure is organized into rows and columns. The rows are labeled 100, 102, 103, 104, and 110. The columns are labeled 112, 114, 116, 117, 118, and 119. The data in the rows is as follows:

Row	112	114	116	117	118	119
100	DVPI	DVCI	00010000	...	H	T
102	DVPI	DVCI	10011111	...	H	T
103	DVPI	DVCI	Output Port #	...		
104	DVPI	DVCI	Output Port #	...		
110	DVPI	DVCI	Output Port #	...		

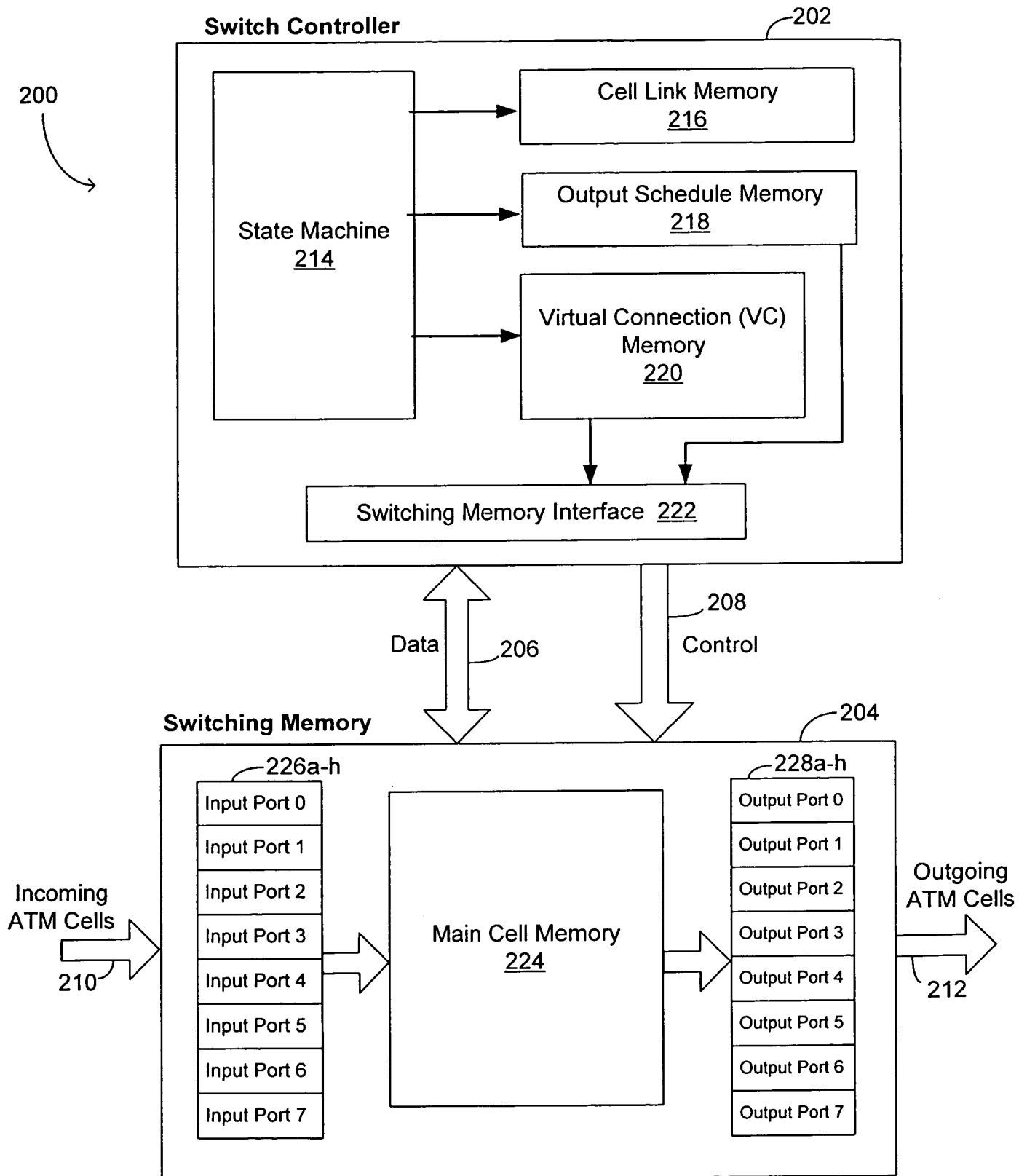


Figure 5

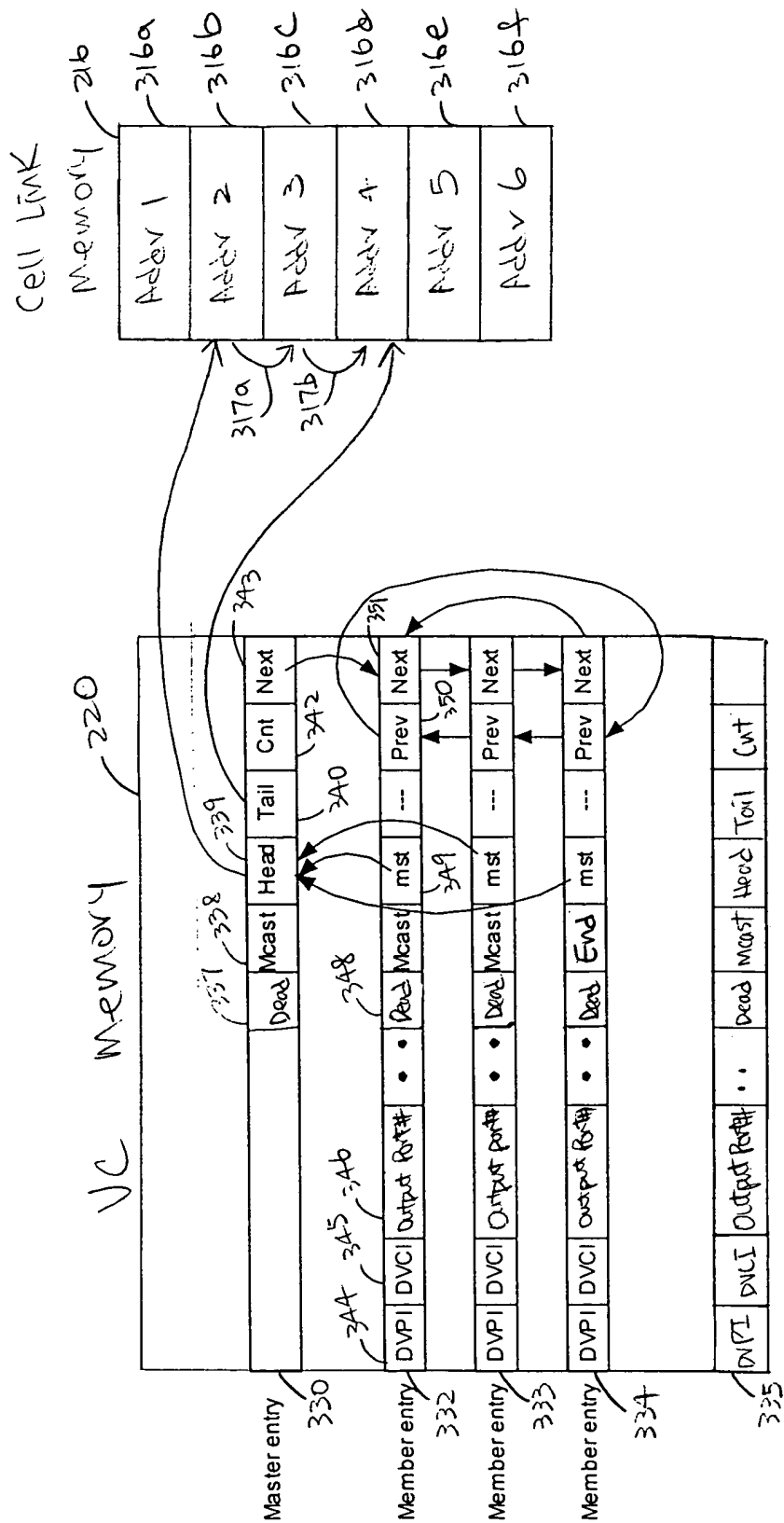


Fig. 6

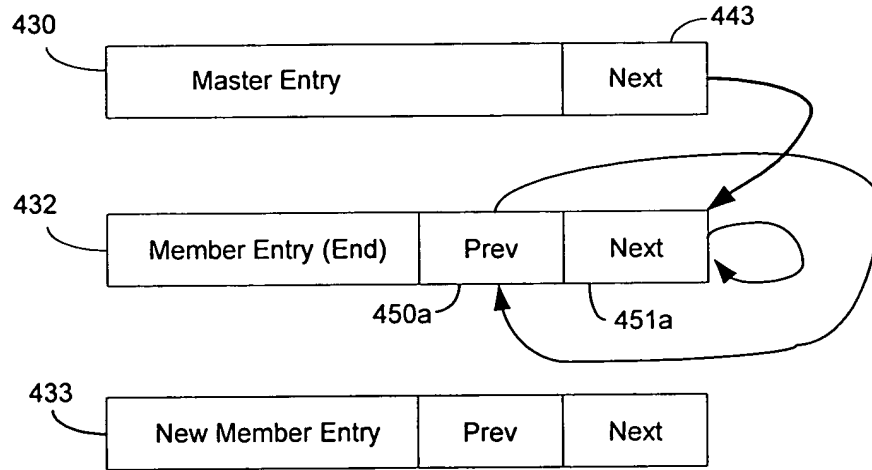


Figure 7a

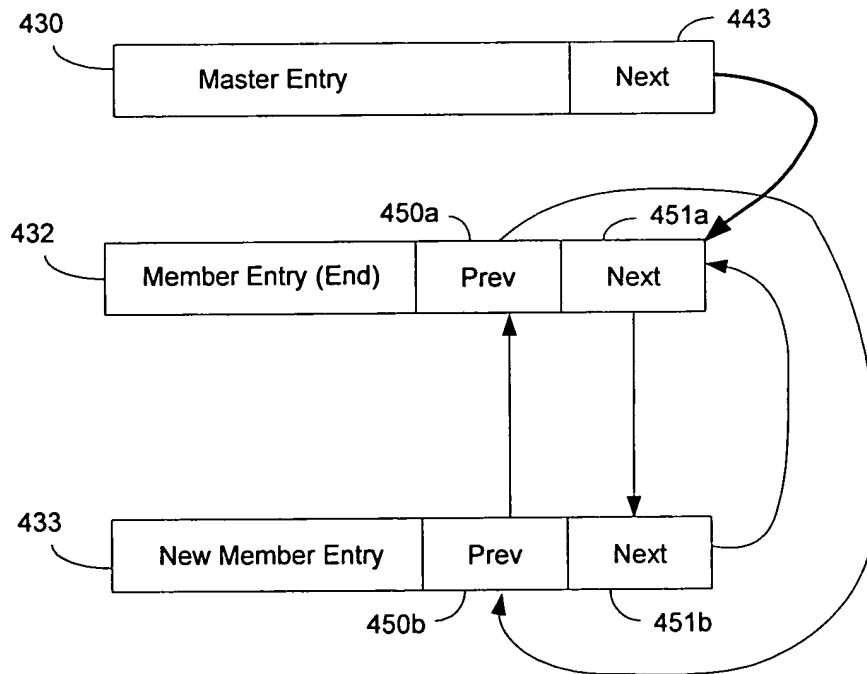


Figure 7b

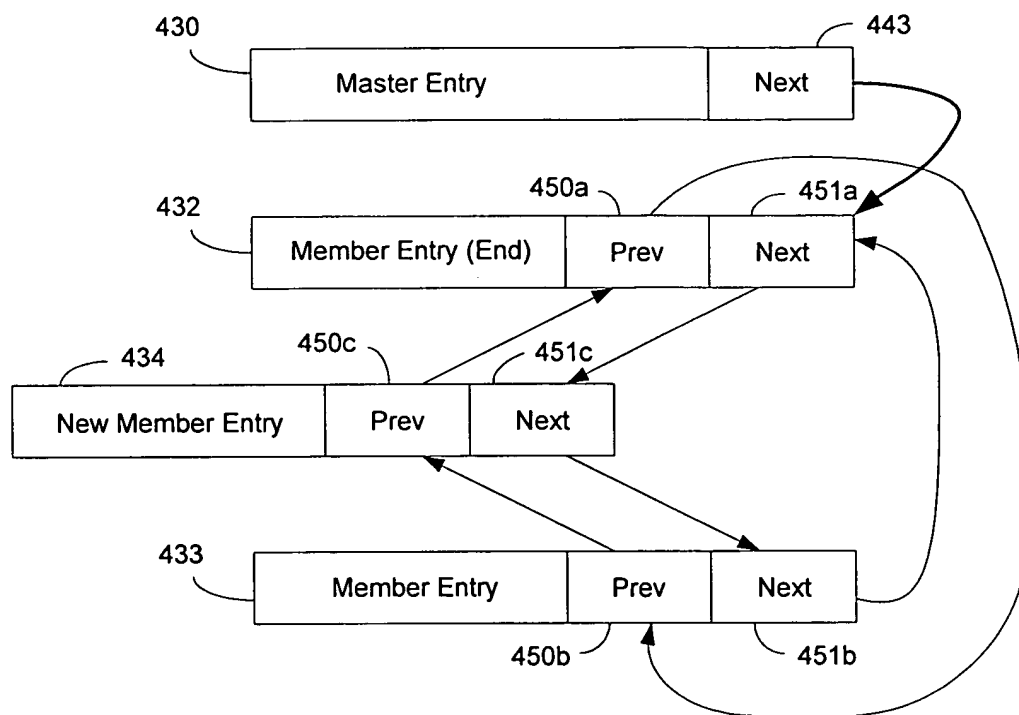


Figure 7c

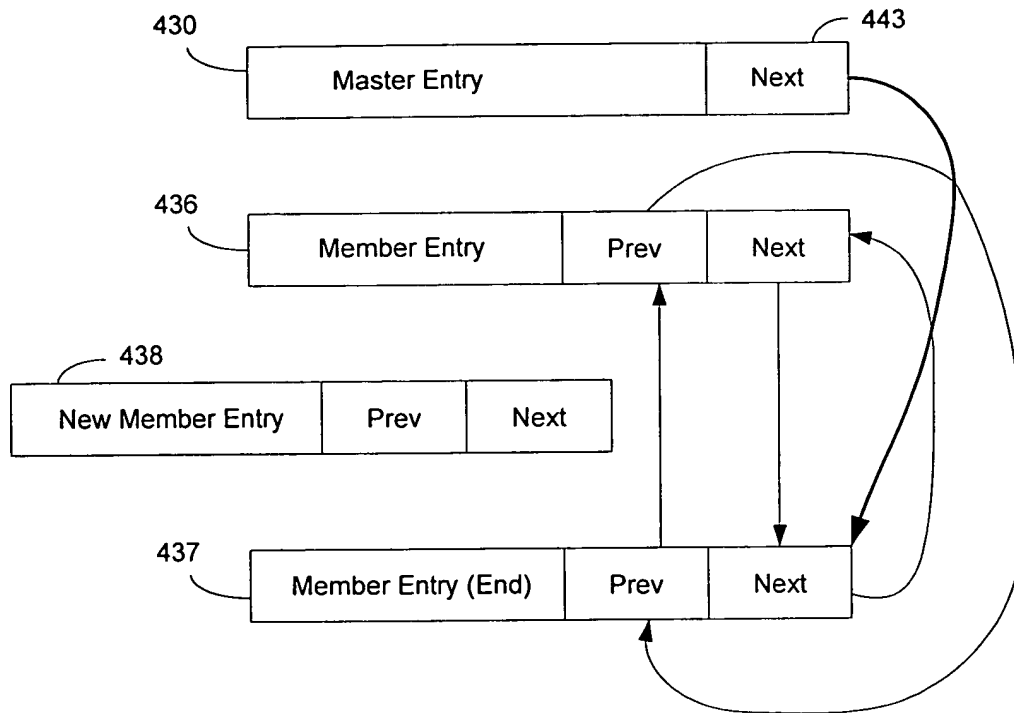


Figure 7d

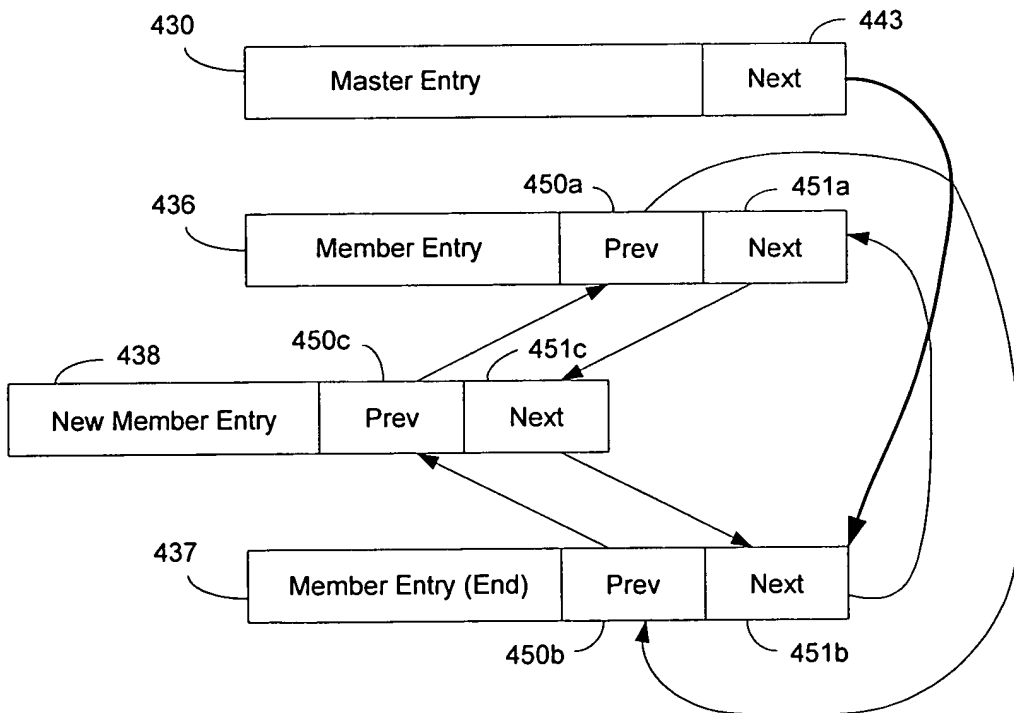


Figure 7e

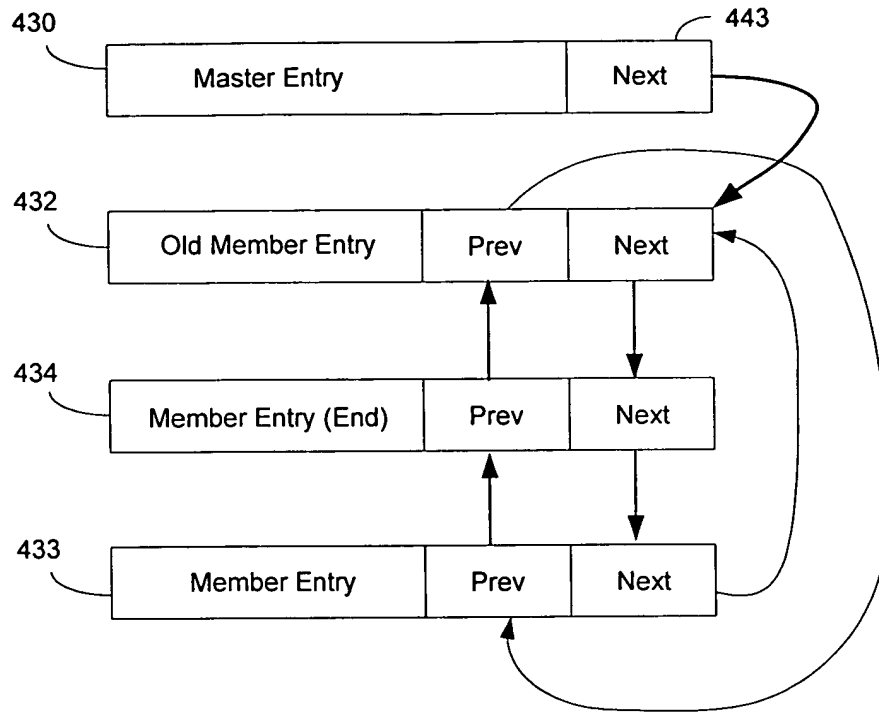


Figure 8a

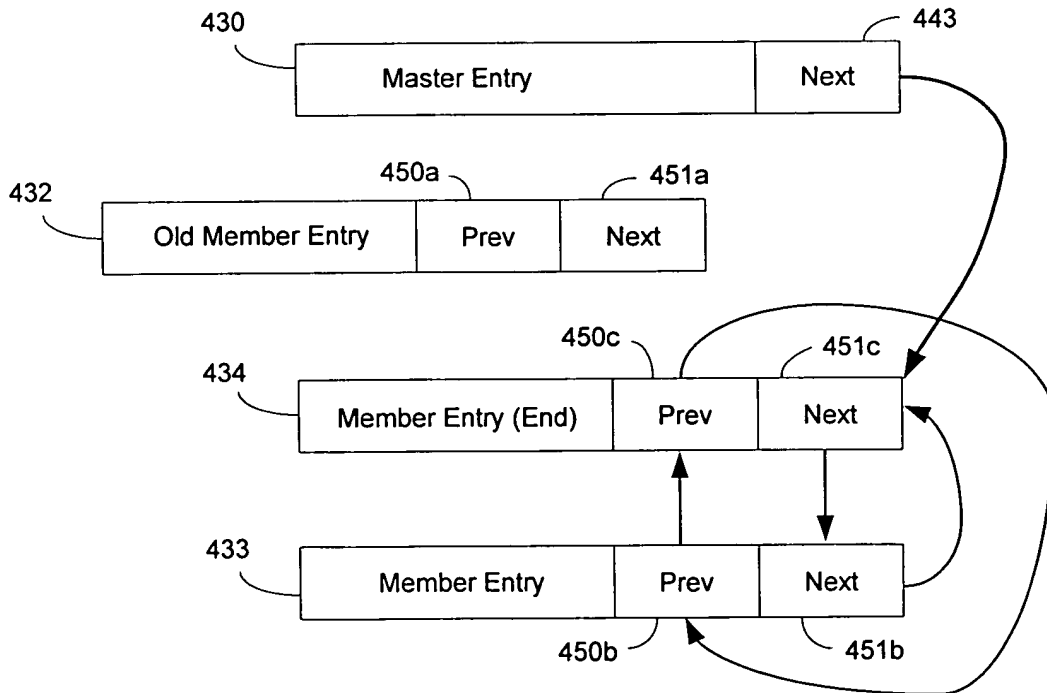


Figure 8b

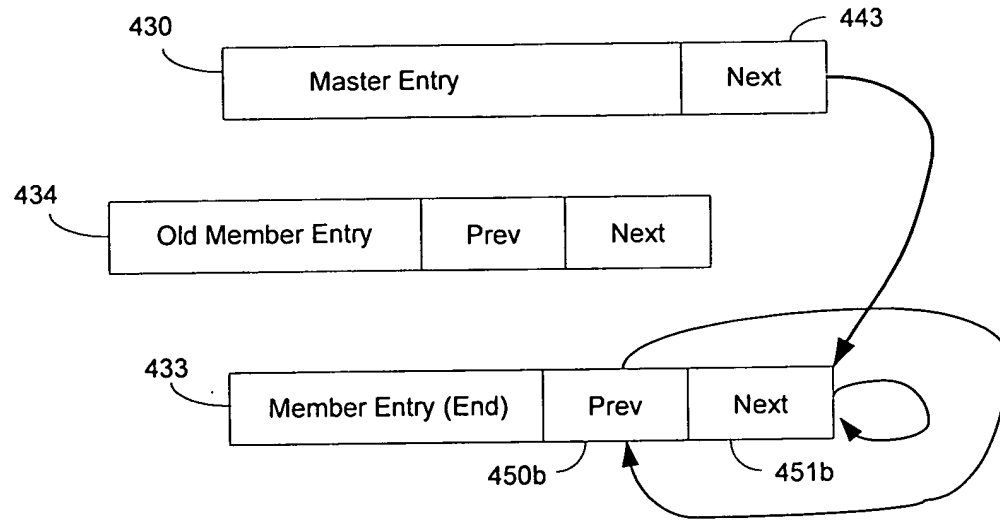


Figure 8c

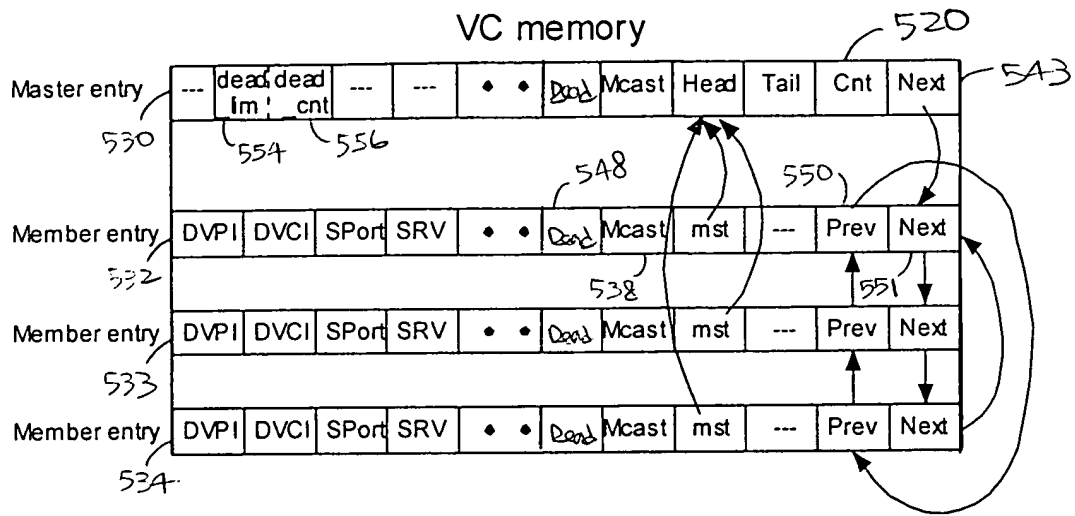


Fig. 9

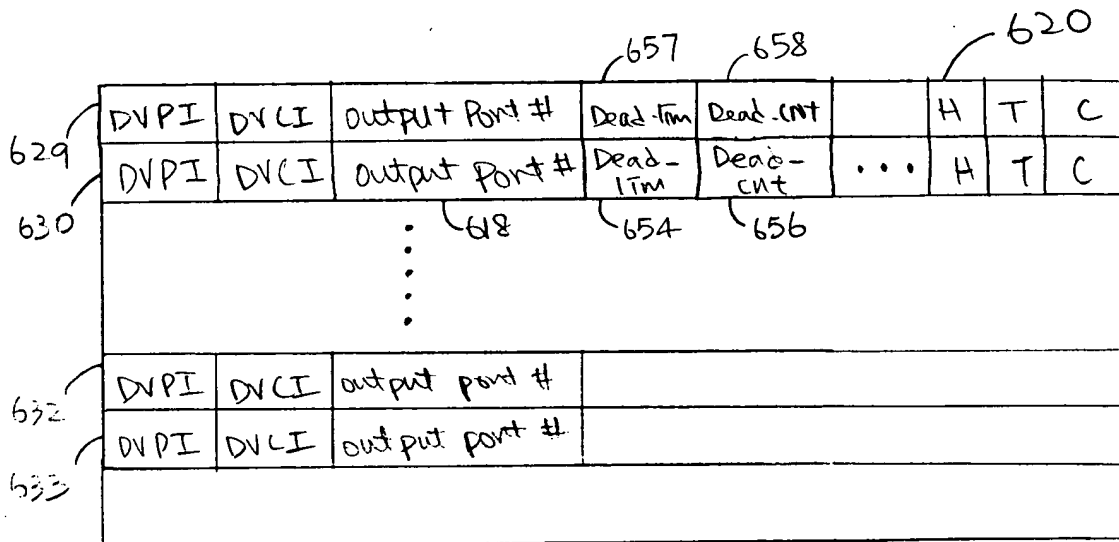


Fig. 10